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Unit 3

Counters

Counters counts the number of clock pulses.

Counter designing:

$2^n \geq N$

n = no. of flip-flop

N = no. of states

eg 1 :- Mod 5 counter

$N = 5$

$2^n \geq N$

$2^n \geq 5$

$n = 3$

eg: Decade counter (Mod-10 counter)

$2^n \geq 10$

$n = 4$

eg:- Design 3-bit counter.

$n = 3$ flip-flop required

$2^n \geq N$

$2^3 \geq 8$

$N = 8$

eg:- Mod 3 Mod 4 Mod 6

Mod 72

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$2^n \geq 72$

$n = 7$

eg:- $f = 12\,KHz$ → [Mod 3 Mod 4] → $f_{out} = ?$

Mod 3 Mod 4 = Mod 12

$$\frac{f}{N} = \frac{12}{12} = 1\,KHz$$

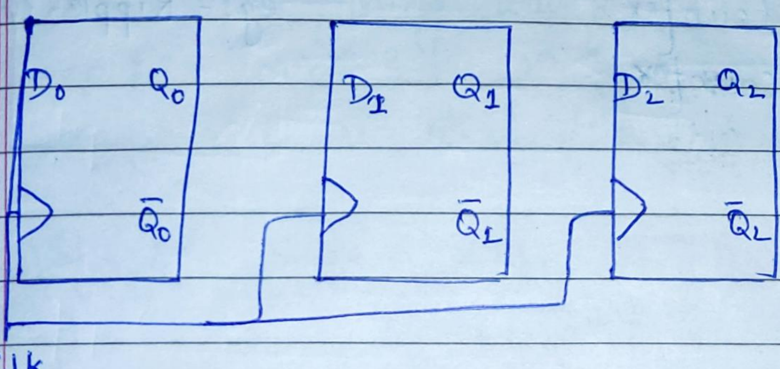
Counters

Synchronous Counters

1. All the flip-flop are applied or connected with the same clock.

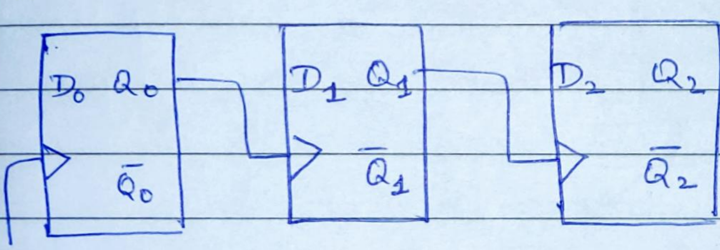
Asynchronous Counter

All the flip-flops are applied or connected with different clock



clk

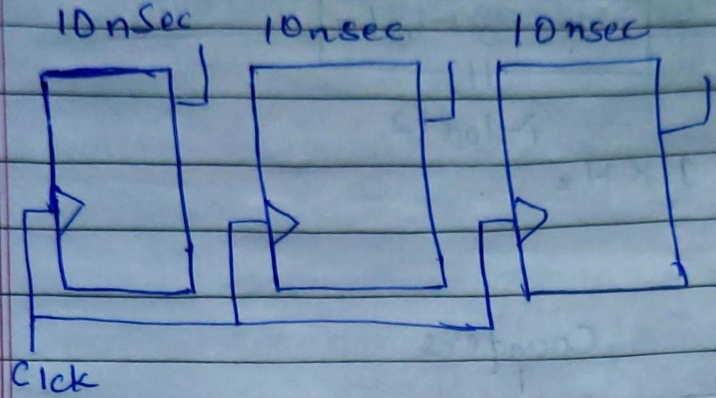
(Synchronous)



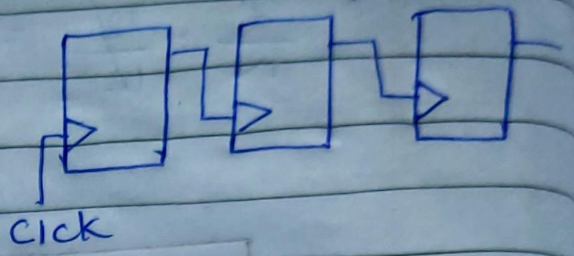
clck

(Asynchronous)

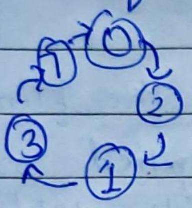
Synchronous	Asynchronous
② fast	slow
③ $T_{clk} \geq t_{pd\,ff}$	$T_{clk} \geq n\,t_{pd\,ff}$ n = no. of flip-flops

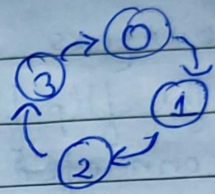


delay of 30 n sec



Synchronous	Asynchronous
④ Random sequence possible	Fixed sequence





Synchronous	Asynchronous
⑤ eg:- Johnson Counter Ring counter	eg:- Ripple Counter.

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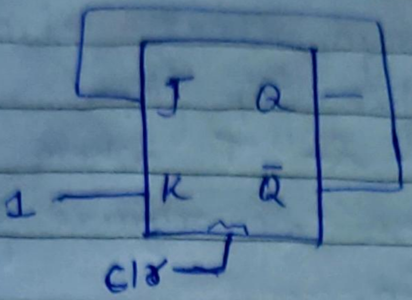
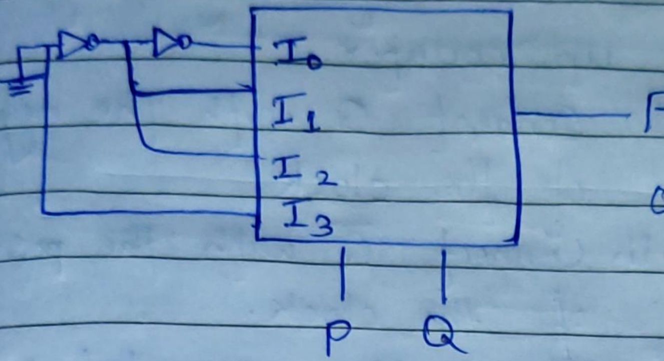


after 6 clck pulse

① 011011 ③ 010100

② 010110 ④ 010101



① F = AND (P, Q)

② F = OR (P, Q)

③ F = XOR (P, Q)

④ F = Xnor (P, Q)

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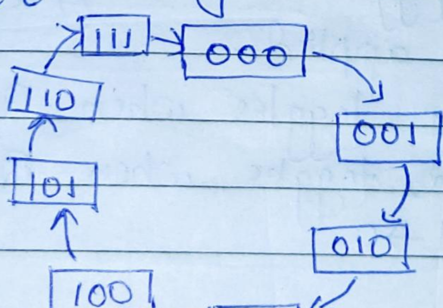
Q Design asynchronous divide by 8 up counter and draw its timing waveforms?

⇒ Step 1 :- mod-8 , $2^n \geq N$, $2^n \geq 8$, $2^n \geq 2^3$, n = 3

n = no. of flip flops & N = no. of states

Step 2 :- State Design :-



Step 3:- Fact 1 - All asynchronous circuit are designed by two flip-flops.
J-K & T where J, K = 1 & T = 1 because we require there toggling action.

Fact 2 - in order to design asynchronous up counter.

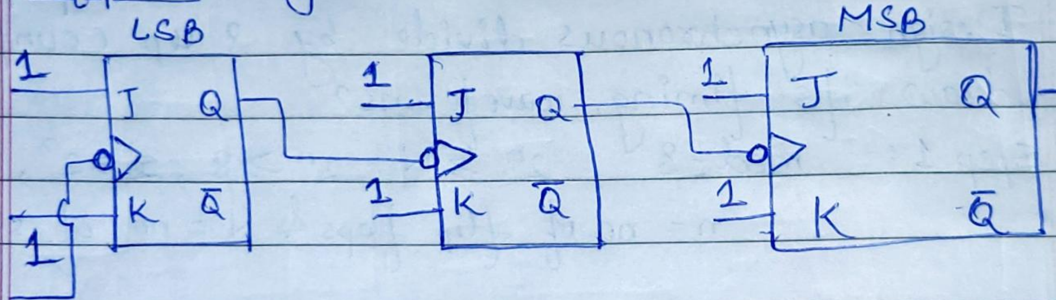
(i) Connect Q with the negative edge of the clock.

OR

(ii) Connect $\bar{Q}$ with the positive edge of the clock.

Fact 3 - The flip-flop connected to first clock acts as LSB.

Step 4:- Design



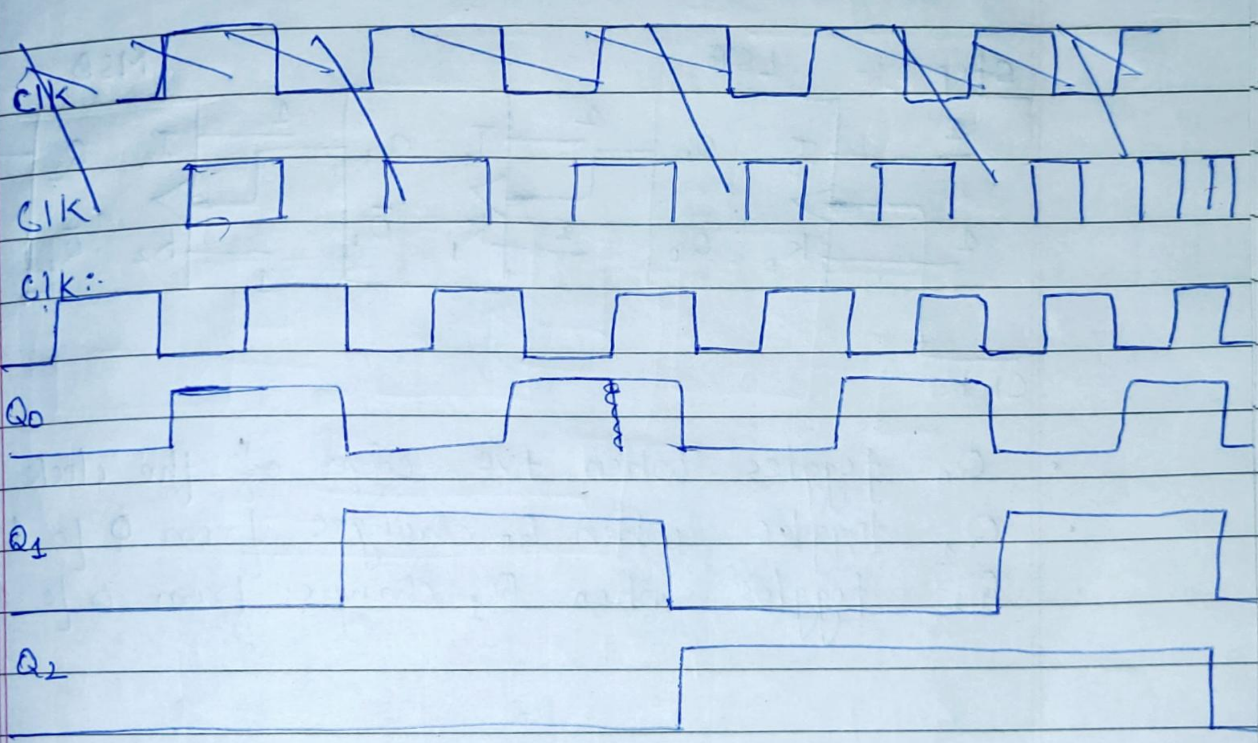
Fact 4 - (i) Q_0 toggles when negative edge of the clk is applied.

(ii) Q_1 toggles when Q_0 changes from $1 \to 0$.

(iii) Q_2 toggles when Q_1 changes from $1 \to 0$.

Step 5:- Truth-table

Clk	(MSB) Q_2	Q_1	Q_0 (LSB)
↑0	0	0	0
↓1	0	0	1
↓2	0	1	0
↓3	0	1	1
↓4	1	0	0
↓5	1	0	1
↓6	1	1	0
↓7	1	1	1
↓8	0	0	0



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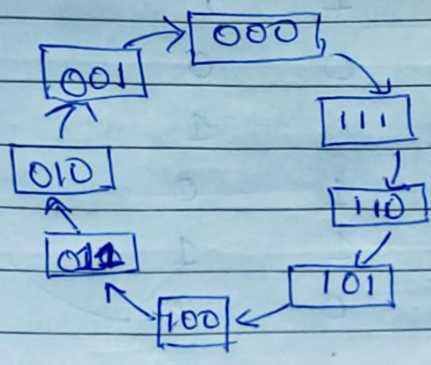
Q Design asynchronous divide by 8 down counter & draw its timing waveforms.

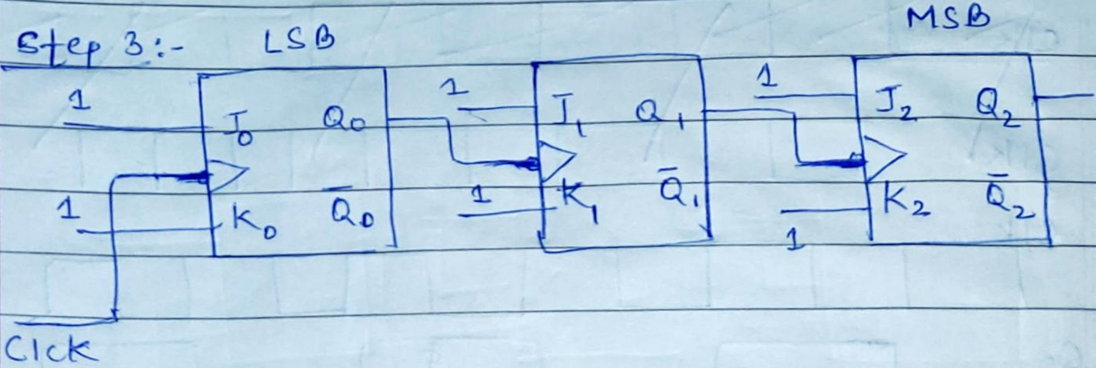
Step 1 :-

$2^n \geq N$, $2^n \geq 8$, $2^n \geq 2^3$, $n = 3$

Step 2 :- State diagram



Step 3 :-



- Q_0 toggles when +ve edge of the clock occurs
- Q_1 toggles when Q_0 changes from 0 to 1
- Q_2 toggles when Q_1 changes from 0 to 1

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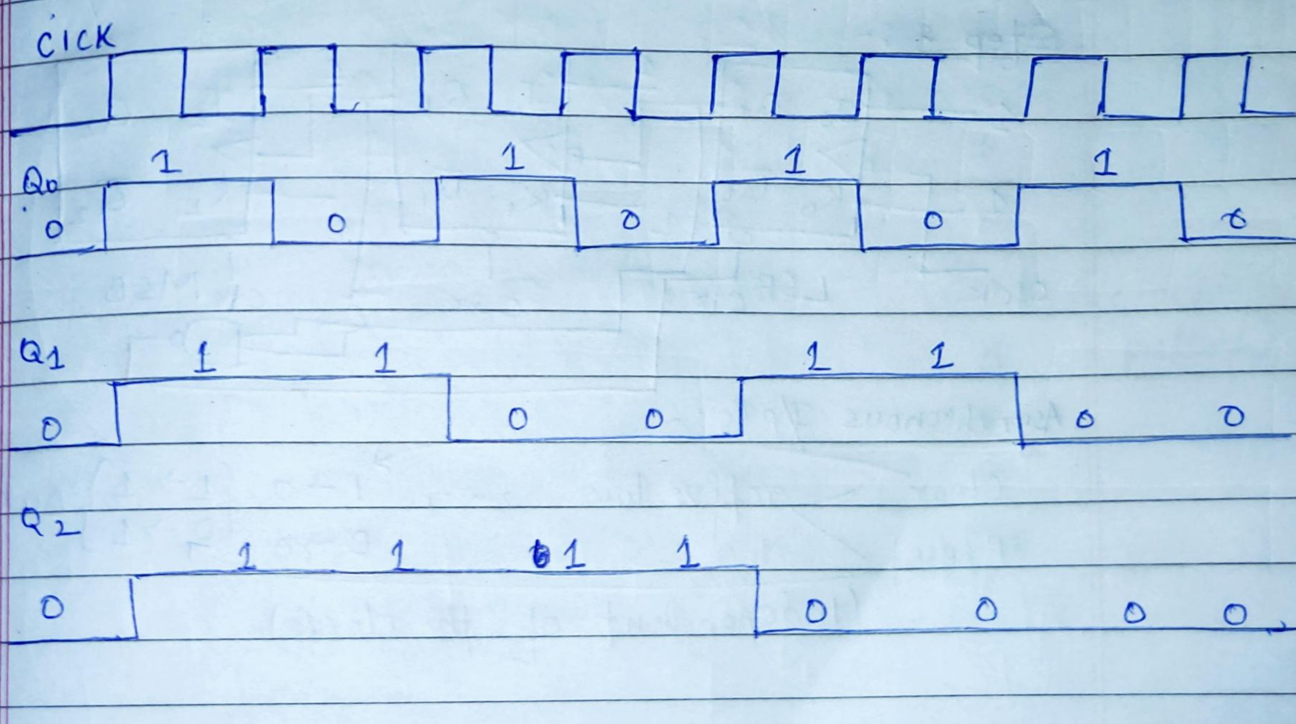
Step 4:- Truth-table

Clk	(MSB) Q_2	Q_1	(LSB) Q_0
0	0	0	0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
8	0	0	0

Step 5:- Waveform



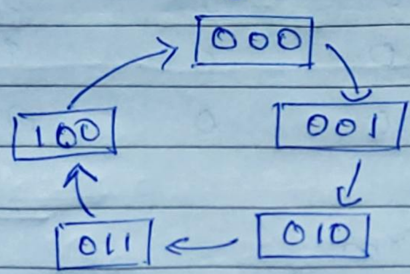
Q. Design and implement mod-5 asynchronous counter? (by default up counter)

Step 1 :- $2^n \geq N$

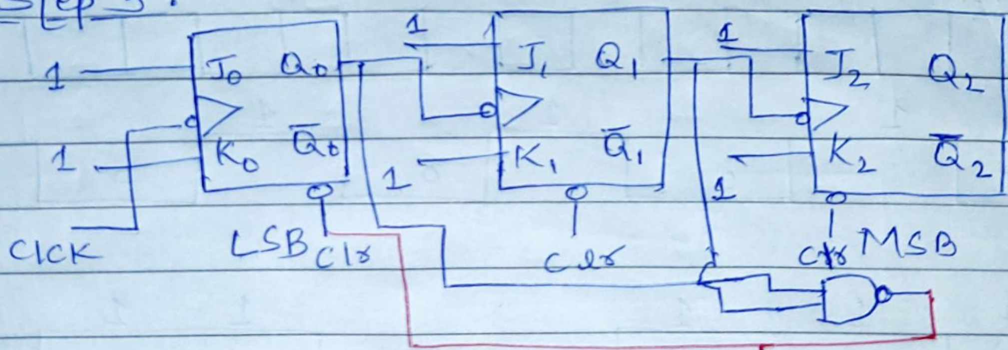
$2^n \geq 5$

$n = 3$

Step 2 :- State diagram



Step 3 :-



Asynchronous I/P's :-

Clear — active low i.e., 1 → 0 {1 → 1} output

Preset — 0 → 0 {0 → 1}

(Independent of the clock)

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Registers

- Registers are used to store group of bits
- In order to store n-bit of data, minimum 'n' no. of flip-flops are required.

Shift Registers

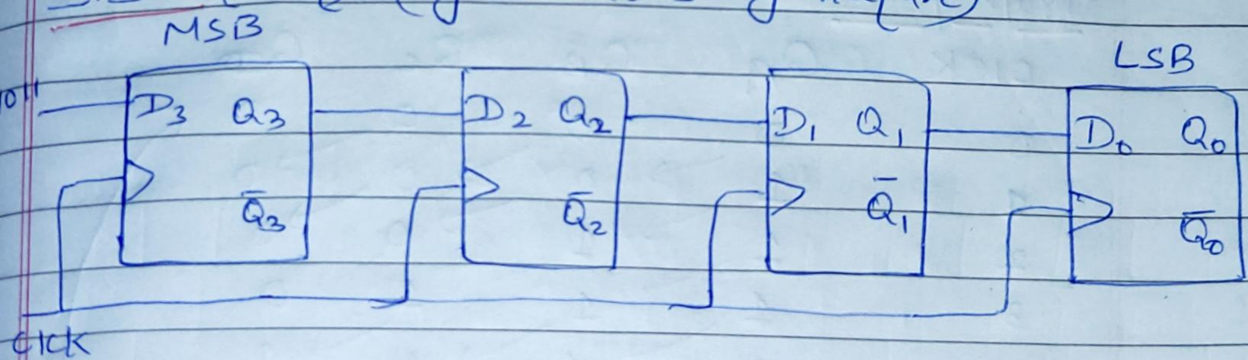
SISO (Serial In Serial Out)

SIPO (Serial In Parallel Out)

PISO (Parallel In Serial Out)

PIPO (Parallel In Parallel Out)

SISO (4 bit) (synchronous by nature)



Data	Q_3	Q_2	Q_1	Q_0	Clck (4 clock pulses)
1011	0	0	0	0	0
	1	0	0	0	↑
	1	1	0	0	↑
	0	1	1	0	↑
	1	0	1	1	↑

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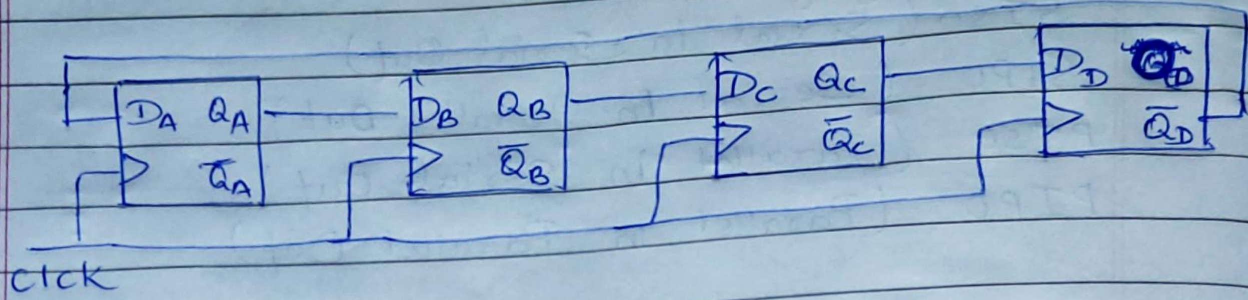
Johnson Counter / Twisted Ring Counter / Switched Tail Counter

1. Synchronous Counter
2. Flip-flops are connected to same clock.
3. SISO - shift register with feedback



Truth-table:-

Clck	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

- After 8 clock pulses it starts repeating itself
- After every $2n$ clock pulse it repeat itself
- Total no. of states $= 2^n$ where unused states $= 2^n - 2n$

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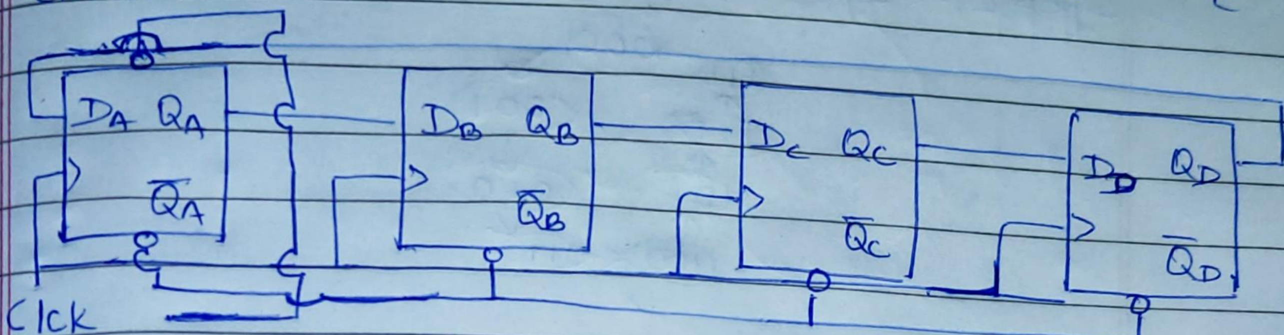
Ring Counter

1. Synchronous Counter
2. Shift register behaviour (SISO) with feedback
3. In ring counter the very first flip-flop o/p is going to be ~~one~~. 1 & it will rotate with clock.



Preset	clck	Q_A	Q_B	Q_C	Q_D	Clr
1	0	0	0	0	0	0
0	~~1~~ 0	1	0	0	0	1
1	~~2~~ 1	0	1	0	0	1
1	~~3~~ 2	0	0	1	0	1
1	~~4~~ 3	0	0	0	1	1
1	~~4~~ 4	1	0	0	0	1

After 4 clock pulses it repeats itself.

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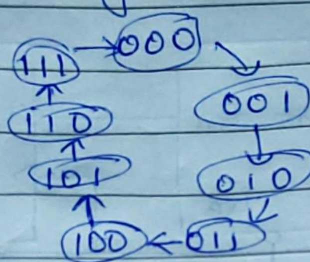
Designing of synchronous counter

Q Mod-8 synchronous Counter using J-K flipflop

Step 1 :- $2^n \geq N \Rightarrow 2^n \geq 8 \Rightarrow n = 3$

Step 2 :- State diagram



Step 3 :- ~~Exit~~ Excitation table of JK flip flop

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Step 4 :- Counter table

J_CK_C	Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_AK_A	J_BK_B
1X	0	0	0	0	0	1	0X	0X
X1	0	0	1	0	1	0	0X	1X
1X	0	1	0	0	1	1	0X	X0
X1	0	1	1	1	0	0	1X	X1
1X	1	0	0	1	0	1	X0	0X

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Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	$J_A K_A$	$J_B K_B$	$J_C K_C$
1	0	1	1	1	0	X0	1X	X1
1	1	0	1	1	1	X0	X0	1X
1	1	1	0	0	0	X1	X1	X1

Step 5 :- K-Map

J_A =

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	(0)	(1)	1 (3)	(2)
1	X (4)	X (5)	X (7)	X (6)

Q_A	Q_B	Q_C
0	1	1
1	1	1
X	Q_B	Q_C

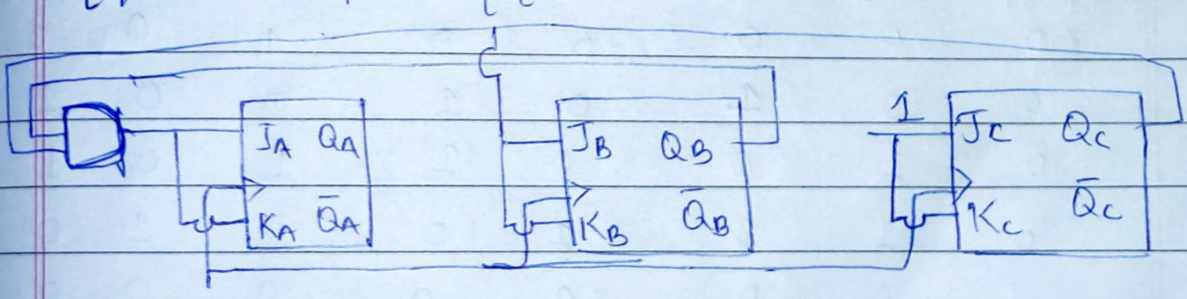
K_A =

$Q_A \backslash Q_B Q_C$	00	01	11	10
0	X (0)	X (1)	X (3)	X (2)
1	(4)	X (5)	1 (7)	(6)

$K_A = Q_B Q_C$ $\quad J_B = Q_C$ $\quad J_C = 1$

$K_B = Q_C$ $\quad K_C = 1$

Step 6 :- Implementation

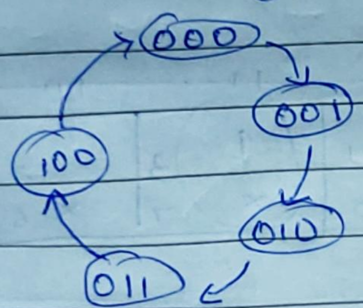


clck

Q. Mod 5 synchronous counter

Step 1:- $2^n \geq N \Rightarrow 2^n \geq 5 \Rightarrow n = 3$

Step 2:- State diagram



Step 3:- Excitation table of D

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Step 4:- Counter table

Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	D_A	D_B	D_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	0	0	0	0	0	0

Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	D_A	D_B	D_C
1	0	1	x	x	x	x ⓪	x	x
1	1	0	x	x	x	x ⓪	x	x
1	1	1	x	x	x	x	x	x

Step 5:- K-Map

$D_A = Q_B Q_C$ 0 → $Q_A = 0$

$D_B = Q_C$ 0 → $Q_B = 0$

$D_C = \bar{Q}_A \bar{Q}_C$ 0 → $Q_C = 0$

1

000 → 001 → 010

$Q_A Q_B Q_C$

100 → 000

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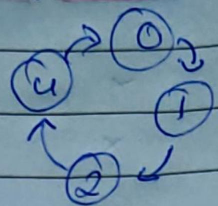
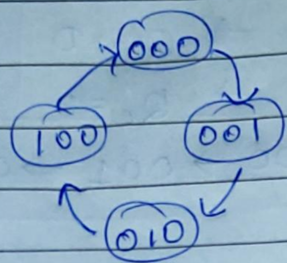
Random sequence using T flip flop



Step 1:- Mod 5 ⇒ $2^n \geq N \Rightarrow 2^n \geq 5 \Rightarrow n = 3$

Step 2:-



Step 3:- Excitation Table:-

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Step 4:- Counter Table:-

Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	T_A	T_B	T_C
0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1	1
0	1	0	1	0	0	1	1	0
0	1	1	x	x	x	x	x	x

Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	T_A	T_B	T_C
1	0	0	0	0	0	1	0	0
1	0	1	x	x	x	x	x	x
1	1	0	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x
						x	x	x

Step 5:- K-Map

$T_A = Q_A + Q_B$

$T_B = Q_C + Q_B$

$T_C = Q_A' Q_B'$

Implementation (Step 6):-